CLAIMS

What is claimed is:

1. A memory system, comprising:

a memory hub controller adapted to provide memory command packets including information to access memory devices;

a memory module having a plurality of memory devices coupled to a memory hub, the memory hub adapted to receive memory command packets and access the memory devices according to the memory command packets and further adapted to provide memory responses in response thereto;

a first portion of a memory bus coupled to the memory hub controller and the memory hub on which the memory command packets from the memory hub controller are provided to the memory hub of the memory module and memory responses are provided to the memory hub controller;

an expansion module having a processor circuit adapted to provide memory command packets including information to access the memory devices of the memory module and further adapted to process data included in the memory responses from the memory hub; and

a second portion of the memory bus coupled to the memory hub of the memory module and the processor circuit of the expansion module on which the memory command packets from the processor circuit are provided to the memory hub of the memory module and memory responses are provided to the processor circuit.

2. The memory system of claim 1 wherein the first and second portions of the memory bus comprise:

a downstream bus having a first portion coupled between the memory hub controller and the memory hub to which memory command packets from the memory hub controller to the memory hub are coupled and further having a second

portion coupled between the memory hub and the processor circuit to which memory responses from the memory hub to the processor circuit are coupled; and

an upstream bus having a first portion coupled between the memory hub controller and the memory hub to which memory responses from the memory hub to the memory hub controller are coupled and further having a second portion coupled between the memory hub and the processor circuit to which memory command packets from the processor circuit to the memory hub are coupled.

3. The memory system of claim 1 wherein the expansion module further comprises:

a plurality of memory devices adapted to provide a local memory space; and

a local memory bus coupled to the processor circuit and the plurality of memory devices through which the processor circuit accesses the local memory space.

4. The memory system of claim 1 wherein the processor circuit of the expansion module comprises a graphics controller to process graphics data stored in the memory devices of the memory module.

5. The memory system of claim 1 wherein the processor circuit of the expansion module comprises an input/output processor to process input data and store the same in the memory devices of the memory module and to process output data stored in the memory devices of the memory module.

6. The memory system of claim 1 wherein the memory hub of the memory module comprises:

a switch circuit having a plurality of switch nodes and adapted to couple any one switch node to another switch node;

a plurality of link interface circuits, each link interface circuit having a first node coupled to a respective one of the plurality of switch nodes and further having a second node coupled to either the first or second portions of the memory bus, each link interface circuit coupling signals from its first node to its second node;

a memory controller coupled to a switch node of the switch circuit to receive memory command packets and translate the same into memory device command signals; and

a local memory bus coupled to the memory controller and the memory devices on which the memory device command signals are provided.

7. The memory system of claim 6 wherein the plurality of link interface circuits comprise:

a first pair of link interface circuits having a downstream link interface coupled to a first portion of a downstream bus and further having an upstream link interface coupled to a first portion of an upstream bus, both the first portions of the downstream and upstream buses coupled to the memory hub controller and the memory hub; and

a second pair of link interface circuits having a downstream link interface coupled to a second portion of the downstream bus and further having an upstream link interface coupled to a second portion of the upstream bus, both the second portions of the downstream and upstream buses coupled to the memory hub and the processor circuit.

8. The memory system of claim 1 wherein the memory devices of the memory module comprise synchronous dynamic random access memory devices.

9. A memory system, comprising:

first and second memory modules, each memory module having a respective plurality of memory devices and a respective memory hub coupled to the respective plurality of memory devices, the respective memory hubs adapted to receive memory requests for accessing memory locations in the respective plurality of memory devices and provide memory responses in response to receiving the memory requests;

first and second expansion modules, each expansion module having a respective processor circuit adapted to provide memory requests to the memory hubs to access memory locations in the respective plurality of memory devices and receive memory responses from the memory hubs;

a memory hub controller adapted to provide memory requests to the memory modules to the memory hubs to access memory locations in the respective plurality of memory devices and receive memory responses from the memory hubs; and

a memory bus coupled to the first and second memory hubs, the first and second processor circuits and the memory hub controller, the memory bus configured to couple memory requests to the memory modules and couple memory responses to the memory hub controller and the first and second processor circuits.

10. The memory system of claim 9, further comprising a third memory module having a third plurality of memory devices and a third memory hub coupled to the third plurality of memory devices and further coupled to the memory bus in a point-to-point arrangement, the point-to-point arrangement coupling the memory hub controller to the first memory hub of the first memory module, coupling the first memory hub to the second memory hub of the second memory module, coupling the second memory hub to the first processor circuit of the first expansion module, coupling the first processor circuit to the third memory hub of the third memory module; and coupling the third memory hub to the second processor circuit of the second expansion module.

11. The memory system of claim 9 wherein the memory bus comprises a pair of unidirectional buses having portions coupled between the first and second memory hubs, the first and second processor circuits and the memory hub controller to provide the point-to-point arrangement.

12. The memory system of claim 9 wherein at least one of the first and second expansion modules further comprises:

a plurality of memory devices adapted to provide a local memory space; and

a local memory bus coupled to the respective processor circuit and the respective plurality of memory devices through which the processor circuit accesses the local memory space.

13. The memory system of claim 9 wherein the processor circuit of at least one of the first and second expansion modules comprises a graphics controller to process graphics data stored in the memory devices of at least one of the memory modules.

14. The memory system of claim 9 wherein the processor circuit of at least one of the first and second expansion modules comprises an input/output processor to process input data and store the same in the memory devices of at least one of the memory modules and to process output data stored in the memory devices of the memory module.

15. The memory system of claim 9 wherein the memory hub of at least one of the memory modules comprises:

a switch circuit having a plurality of switch nodes and adapted to couple any one switch node to another switch node;

a plurality of link interface circuits, each link interface circuit having a first node coupled to a respective one of the plurality of switch nodes and further having a second node coupled to the memory bus, each link interface circuit coupling signals from its first node to its second node;

a memory controller coupled to a switch node of the switch circuit to receive memory requests and translate the same into memory device command signals; and

a local memory bus coupled to the memory controller and the memory devices on which the memory device command signals are provided.

16. The memory system of claim 15 wherein the memory bus comprises a unidirectional downstream bus and a unidirectional upstream bus, and the plurality of link interface circuits comprise:

a first pair of link interface circuits having a downstream link interface coupled to a first portion of the downstream bus and further having an upstream link interface coupled to a first portion of the upstream bus; and

a second pair of link interface circuits having a downstream link interface coupled to a second portion of the downstream bus and further having an upstream link interface coupled to a second portion of the upstream bus.

17. The memory system of claim 9 wherein the memory devices of the memory module comprise synchronous dynamic random access memory devices.

18. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a peripheral device port, the system controller further comprising a memory hub

controller coupled to a system memory port and adapted to provide memory command packets including information to access memory devices;

a memory module having a plurality of memory devices coupled to a memory hub, the memory hub adapted to receive memory command packets and access the memory devices according to the memory command packets and further adapted to provide memory responses in response thereto;

a first portion of a memory bus coupled to the system memory port and the memory hub on which the memory command packets from the memory hub controller are provided to the memory hub of the memory module and memory responses are provided to the memory hub controller;

an expansion module having a processor circuit adapted to provide memory command packets including information to access the memory devices of the memory module and further adapted to process data included in the memory responses from the memory hub; and

a second portion of the memory bus coupled to the memory hub of the memory module and the processor circuit of the expansion module on which the memory command packets from the processor circuit are provided to the memory hub of the memory module and memory responses are provided to the processor circuit.

19. The processor-based system of claim 18, further comprising at least one peripheral device coupled to the peripheral device port of the system controller;

20. The processor-based system of claim 18 wherein the first and second portions of the memory bus comprise:

a downstream bus having a first portion coupled between the memory hub controller and the memory hub to which memory command packets from the memory hub controller to the memory hub are coupled and further having a second

portion coupled between the memory hub and the processor circuit to which memory responses from the memory hub to the processor circuit are coupled; and

an upstream bus having a first portion coupled between the memory hub controller and the memory hub to which memory responses from the memory hub to the memory hub controller are coupled and further having a second portion coupled between the memory hub and the processor circuit to which memory command packets from the processor circuit to the memory hub are coupled.

21. The processor-based system of claim 18 wherein the expansion module further comprises:

a plurality of memory devices adapted to provide a local memory space; and

a local memory bus coupled to the processor circuit and the plurality of memory devices through which the processor circuit accesses the local memory space.

22. The processor-based system of claim 18 wherein the processor circuit of the expansion module comprises a graphics controller to process graphics data stored in the memory devices of the memory module.

23. The processor-based system of claim 18 wherein the processor circuit of the expansion module comprises an input/output processor to process input data and store the same in the memory devices of the memory module and to process output data stored in the memory devices of the memory module.

24. The processor-based system of claim 18 wherein the memory hub of the memory module comprises:

a switch circuit having a plurality of switch nodes and adapted to couple any one switch node to another switch node;

a plurality of link interface circuits, each link interface circuit having a first node coupled to a respective one of the plurality of switch nodes and further having a second node coupled to either the first or second portions of the memory bus, each link interface circuit coupling signals from its first node to its second node;

a memory controller coupled to a switch node of the switch circuit to receive memory command packets and translate the same into memory device command signals; and

a local memory bus coupled to the memory controller and the memory devices on which the memory device command signals are provided.

25. The processor-based system of claim 24 wherein the plurality of link interface circuits comprise:

a first pair of link interface circuits having a downstream link interface coupled to a first portion of a downstream bus and further having an upstream link interface coupled to a first portion of an upstream bus, both the first portions of the downstream and upstream buses coupled to the memory hub controller and the memory hub; and

a second pair of link interface circuits having a downstream link interface coupled to a second portion of the downstream bus and further having an upstream link interface coupled to a second portion of the upstream bus, both the second portions of the downstream and upstream buses coupled to the memory hub and the processor circuit.

26. The processor-based system of claim 18 wherein the memory devices of the memory module comprise synchronous dynamic random access memory devices.

27. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a peripheral device port, the system controller further comprising a memory hub controller coupled to a system memory port and adapted to provide memory command packets including information to access memory devices;

first and second memory modules, each memory module having a respective plurality of memory devices and a respective memory hub coupled to the respective plurality of memory devices, the respective memory hubs adapted to receive memory requests for accessing memory locations in the respective plurality of memory devices and provide memory responses in response to receiving the memory requests;

first and second expansion modules, each expansion module having a respective processor circuit adapted to provide memory requests to the memory hubs to access memory locations in the respective plurality of memory devices and receive memory responses from the memory hubs;

a memory hub controller adapted to provide memory requests to the memory modules to the memory hubs to access memory locations in the respective plurality of memory devices and receive memory responses from the memory hubs; and

a memory bus coupled to the first and second memory hubs, the first and second processor circuits and the system memory port, the memory bus configured to couple memory requests to the memory modules and couple memory responses to the memory hub controller and the first and second processor circuits.

28. The processor-based system of claim 27, further comprising at least one peripheral device coupled to the peripheral device port of the system controller;

29. The processor-based system of claim 27, further comprising a third memory module having a third plurality of memory devices and a third memory hub coupled to the third plurality of memory devices and further coupled to the memory bus in a point-to-point arrangement, the point-to-point arrangement coupling the memory hub controller to the first memory hub of the first memory module, coupling the first memory hub to the second memory hub of the second memory module, coupling the second memory hub to the first processor circuit of the first expansion module, coupling the first processor circuit to the third memory hub of the third memory module; and coupling the third memory hub to the second processor circuit of the second expansion module.

30. The processor-based system of claim 27 wherein the memory bus comprises a pair of unidirectional buses having portions coupled between the first and second memory hubs, the first and second processor circuits and the memory hub controller to provide the point-to-point arrangement.

31. The processor-based system of claim 27 wherein at least one of the first and second expansion modules further comprises:

a plurality of memory devices adapted to provide a local memory space; and

a local memory bus coupled to the respective processor circuit and the respective plurality of memory devices through which the processor circuit accesses the local memory space.

32. The processor-based system of claim 27 wherein the processor circuit of at least one of the first and second expansion modules comprises a graphics controller to process graphics data stored in the memory devices of at least one of the memory modules.

33. The processor-based system of claim 27 wherein the processor circuit of at least one of the first and second expansion modules comprises an input/output processor to process input data and store the same in the memory devices of at least one of the memory modules and to process output data stored in the memory devices of the memory module.

34. The processor-based system of claim 27 wherein the memory hub of at least one of the memory modules comprises:

a switch circuit having a plurality of switch nodes and adapted to couple any one switch node to another switch node;

a plurality of link interface circuits, each link interface circuit having a first node coupled to a respective one of the plurality of switch nodes and further having a second node coupled to the memory bus, each link interface circuit coupling signals from its first node to its second node;

a memory controller coupled to a switch node of the switch circuit to receive memory requests and translate the same into memory device command signals; and

a local memory bus coupled to the memory controller and the memory devices on which the memory device command signals are provided.

35. The processor-based system of claim 34 wherein the memory bus comprises a unidirectional downstream bus and a unidirectional upstream bus, and the plurality of link interface circuits comprise:

a first pair of link interface circuits having a downstream link interface coupled to a first portion of the downstream bus and further having an upstream link interface coupled to a first portion of the upstream bus; and

a second pair of link interface circuits having a downstream link interface coupled to a second portion of the downstream bus and further having an upstream link interface coupled to a second portion of the upstream bus.

36. The processor-based system of claim 27 wherein the memory devices of the memory module comprise synchronous dynamic random access memory devices.

37. A method of configuring a system memory, comprising:

providing a memory module having a plurality of memory devices coupled to a memory hub, the memory hub adapted to receive memory command packets and access the memory devices according to the memory command packets and further adapted to provide memory responses in response thereto;

coupling the memory hub of the memory module to a system controller adapted to provide memory requests to access the memory devices and receive memory responses from the memory hub; and

coupling an expansion module having a processor circuit to the memory hub, the processor circuit adapted to provide memory requests to the memory hub to access the memory devices of the memory module and further adapted to process data included in the memory responses from the memory hub.

38. The method of claim 37 wherein coupling the memory hub of the memory module to the system controller comprises coupling a unidirectional downstream bus to the system controller and the memory hub to which memory requests from the system controller are coupled and further coupling a unidirectional upstream bus to the system controller and the memory hub to which memory responses from the memory hub to the system controller are coupled.

39. The method of claim 37 wherein coupling the expansion module to the memory hub comprises coupling a unidirectional downstream bus to the memory hub and the processor circuit to which memory responses from the memory hub to the processor circuit are coupled and further coupling a unidirectional upstream bus to the processor circuit and the memory hub to which memory requests from the processor circuit to the memory hub are coupled.

40. The method of claim 37 wherein coupling the expansion module having the processor circuit to the memory hub comprises coupling an expansion module having a graphics controller for processing graphics data stored in the memory devices of the memory module.

41. The method of claim 37 wherein coupling the expansion module having the processor circuit to the memory hub comprises coupling an expansion module having an input/output processor adapted to process input data and storing the same in the memory devices of the memory module and further adapted to process output data stored in the memory devices of the memory module.

42. A method of accessing a system memory having first and second memory modules, each memory module having a plurality of memory devices and a respective memory hub coupled to a respective plurality of memory devices, the memory hubs coupled to each other, the method comprising:

generating memory requests by a memory hub controller for access to the plurality of memory devices of the first memory module;

coupling the memory requests from the memory hub controller to the first memory hub;

generating memory requests by a processor circuit of an expansion module coupled to the second memory hub for access to the plurality of memory devices of the second memory module;

coupling the memory requests from the processor circuit to the second memory hub;

generating memory responses by the second memory hub in response to receiving the memory request from the processor circuit; and

coupling the memory responses from the second memory hub to the processor circuit of the expansion module.

43. The method of claim 42 wherein coupling the memory requests from the processor circuit to the second memory hub comprises coupling the memory requests to a unidirectional upstream bus and coupling the memory responses from the second memory hub to the processor circuit comprises coupling the memory requests to a unidirectional downstream bus.

44. The method of claim 42 wherein generating memory responses by the second memory hub comprises:

coupling the memory request to a memory controller coupled to the plurality of memory devices of the second memory module;

translating the memory request into memory device signals coupled to the plurality of memory devices;

retrieving data from the memory devices in response to the memory device signals; and

generating the memory response including the retrieved data.